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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RAMPURIA, SATISH	
ART UNIT	**PAPER NUMBER**
2124	

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/747,019	BERNSTEIN ET AL.	
	Examiner	Art Unit	
	Satish S. Rampuria	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *June 13, 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to the application filed on December 21, 2000.

2. Claims 1-21 are pending.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7, 11 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bates et al., hereinafter called Bates, US Patent No. 6,378,125, in view of Wen et al., hereinafter called Wen, US Patent No. 5,956,514.

As per claims 1, 2, 3 and 4, Bates discloses:

- A method of debugging code that executes in a multithreaded processor (Abstract, "A computer system... method to facilitate debugging of multi-threaded computer program")

- receiving of program instruction from a remote user interface connected to the processor (col. 3, lines 46-45 "obtains instructions, or op code, and data via a network")

- executing a breakpoint routine (col. 6, lines 44 "break point routine") ***if program execution in the selected microengine encounters the breakpoint*** (col. 6, lines 11-14 "break point routine...

hitting (encountered) break point... determination is made... whether... system... contained... the break point table")

- ***and an identification representing (col. 6, lines 19-23*** "the address… exception… found… break point table… then determination is made… address is associated with a thread ID control point")

- ***pausing program execution***. It is interpreted that program must be paused in order to insert the break point.

- ***inserting a breakpoint after a program instruction that matches the program instruction received from the remote user interface*** (col. 3, lines 32-34 "Thread identification... break points... user inserted interruptions to program execution" and col. 7, lines 66-67 "the received thread identifier is compared with each thread identification control point see in the received thread has hit one of the thread identification control point")

- ***resuming program execution*** (col. 5, lines 6-7 "user provides an input that resumes execution of the program")

- ***executing a breakpoint routine*** (col. 6, lines 44 "break point routine") ***if program execution in the selected microengine encounters the breakpoint*** (col. 6, lines 11-14 "break point routine... hitting (encountered) break point... determination is made... whether... system... contained... the break point table")

- ***resuming program execution in the microengine*** (col. 5, lines 6-7 "resumes execution of the program")

Bates did not explicitly disclose plurality of microprocessor and sending interrupt to a selected microengine.

However, Wen discloses a system uses multi processor and interrupt is being sent to the specific processor (Abstract, "Multiple processor application" and col. 6, lines 58-59, "sending an interrupt 0 to a specific processor").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the system uses multi processor and interrupt is being sent to the specific processor as taught by Wen in to the system of breakpoint as taught by Bates. The modification would be obvious because of one of ordinary skill in the art would be motivated to select a processor from multi processor to debug the program.

As per claim 5, the rejection of claim 4 is incorporated and further Bates discloses:

- sending the identification (col. 5, line 6 "user provide (send) an input") ***an interrupt handler*** (col. 5, lines 11-12 "An interrupt handler")

- executing the breakpoint routine (col. 6, lines 44 "break point routine") ***in the micrengine*** (col. 3, lines 44 "includes at least one processor") ***represented by the identification*** (col. 4, lines 58-59 "setting a thread identification control point or a break point")

As per claim 6 and 7, the rejection of claim 1 is incorporated and further Bates discloses:

- the data are representative of the state of the threads in the selected microengine (col. 5, lines 56-58 "This record 47 will include data and to whether the control point is to be a thread identification control point, such as by setting high the thread ID control point flag 54 in FIG. 3")

As per claim 11, the rejection of claim 1 is incorporated and further Bates discloses:

- breakpoint routine resides in a store of a controlling processor. It is interpreted that in order to process the breakpoint routine it must be reside in the processor, i.e., control.

Claim 21 is the product claim corresponding to method claim 1 and rejected under the same reason set forth in connection of the rejection of claim 1 above.

5. Claims 8-10 and 12-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bates, in view of Wen, and further in view of Mitchell, hereinafter called Mitchell, U.S. Patent No. 6,230,119.

As per claim 8, 9, and 10 the rejection of claim 4 incorporated and further Bates did not explicitly disclose using a register with certain bits assigned to particular action:

However, Mitchell discloses a processor using a register with having bits assign to perform certain action (col. 5, lines 63-64 "FIG. 8 illustrates the emulation control register, EMUCON, provided within a data processor" and col. 6, lines 29-31 "The sixth bit is an emulation single step, ESS bit which causes the data processor to only execute single instructions between emulator programme operations" and col. 6, lines 9-13 "The fifth bit

enables execution... EES register inspected... determine whether the breakpoint instruction should actually be executed"). in an analogous system for break point execution in a debugger.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to processor using a register in to perform certain actions as taught by Mitchell in corresponding to the breakpoint processing method for multi processors as taught by the combination system of Bates and Wen. The modification would be obvious because of one of ordinary skill in the art would be motivated to include the registers in the data processor to execute the tasks during debug operations as suggested by Mitchell (col. 2, lines 9-12).

As per claim 12, Bates discloses:

- perform a breakpoint routine residing in a debug library in one of the contexts (col. 7, lines 34-37 "The breakpoint manager routine ... would be performing... corresponding action... regard to the breakpoint table (library)")

- and resume program execution (col. 5, lines 6-7 "resumes execution of the program")

Bates does not explicitly disclose a processor can execute multiple context have a register, a counter, and an arithmetic logic unit.

However, Mitchell discloses ***a processor that can execute multiple contexts*** (col. 3, lines 3-4 "data processor executes emulation instructions (context) using reserved emulation registers") ***a register stack*** (col. 3, line 7-8 "the stack, which may experience some minor and

wholly reversible alterations") ***a program counter for each executing context*** (col. 5, lines 11-12 "program counter and stack used by user executable code") ***an arithmetic logic unit*** (col. 5, line 57-58 "the processing core (also known as an arithmetic logic unit ALU)") ***coupled to the register stack*** (col. 5, lines 60-61 "reserved register... include... stack")

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made the processor including a register, a counter and an arithmetic logic unit as taught by Mitchell in corresponding the breakpoint method as taught by Bates. The modification would be obvious because one of ordinary skill in the art would be motivated to have a processor in the breakpoint method because breakpoint would not be possible if there no processor present.

As per claim 13, the rejection of claim 12 is incorporated and further the combination of the disclosure of Bates and Michelle would include:

- a breakpoint in the context points to the breakpoint routine (col. 5, lines 10-16 "An interrupt handler... passes information regarding... interrupt to the break point manager 30. The break point manager 30...updates the break point table 32... as required... to determine what type of control point was encountered and the associated processing")

As per claim 14, the rejection of claim 12 is incorporated and further the combination of the disclosure of Bates and Michelle would include:

- wherein the breakpoint is inserted into the context in response to a user request received through a remote user interface connected to the processor (col. 3, lines 32-34 "Thread

identification control points and break points are both examples of control points, which are generally user inserted interruptions to program execution")

As per claim 15, the rejection of claim 13 is incorporated and further Mitchell discloses:

- wherein an end of the breakpoint routine points to a program counter of the context (col. 7, lines 54-57 "During execution of the user programme, the programme counter will eventually point to the address 0120 which has the A5 emulation break point instruction written therein in place of the "clear A" instruction")

As per claim 17, the rejection of claim 13 is incorporated and further Bates discloses:

- wherein the breakpoint causes an interrupt (col. 3, lines 37-38 "Thus, the invalid (breakpoint) instruction causes a hardware interrupt")

As per claim 18, the rejection of claim 17 is incorporated and further Bates discloses:

- wherein an interrupt handler services the interrupt (col. 5, lines 11-13 "An interrupt handler, or similar means, passes information regarding the exception or interrupt to the break point manager 30")

As per claim 19, the rejection of claim 18 is incorporated and further Bates discloses:

- wherein the interrupt handler identifies the context from the interrupt (col. 5, lines 15-16 "as required in order to determine what type of control point was encountered and the associated processing")

As per claim 20, the rejection of claim 18 is incorporated and further Bates discloses:

- wherein the interrupt handler identifies a processor identification (col. 5, lines 15-16 "as required in order to determine what type of control point was encountered and the associated processing")

As per claims 3 and 16, the rejection of claims 1 and 12 are incorporated respectively and further Mitchell disclose:

- disabling a processor enable bit associated with the selected microengine (col. 6, lines 9-13 "The fifth bit enables execution... EES register inspected... determine whether the breakpoint instruction should actually be executed").

Bates did not explicitly discloses breakpoint routine perform at a context switch/swap.

However, Wen discloses the context switch at routine (col. 6, lines 42-45 "The processor register context may be switched between application 64 and the monitor software 46 modes by the appropriate one of two routines from the application context switch CSU 66").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of context switch as taught by Wen in corresponding to the break point processing method in the combination system as taught by Bates and Mitchell. The modification would be obvious because of one of ordinary skill in the art would be motivated to switch the processor's attention from one task to another to perform the priority task first.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patent is cited to further show the state of the art with respect to breakpoint method of a program.

US Patent No. 5,838,975 to Abramson et al.

US Patent No. 6,378,124 to Bates et al.

US Patent No. 6,543,049 to Bates et al.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Satish Rampuria whose telephone number is 703-305-8891. The examiner can normally be reached on Monday-Friday from 8:30 A. M. to 5:00 P.M. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Kakali Chaki can be reached at 703-305-9662. The fax number for this group is 703-872-9306.

An inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is 703-305-3900.

Satish S. Rampuria

Patent Examiner

Art Unit 2124

01/26/04

Kakali Chaki

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